What is claimed is:

1. An assembly, comprising:

a die, the die having a body comprising a first material; and

an interposer having a first side and a second side, the die coupled to the first side of the interposer;

wherein the interposer comprises the first material, and the first side is electrically and mechanically coupled to the die.

2. The structure of Claim 1, further comprising circuit elements embedded within the interposer.

3. The structure of Claim 2, wherein circuit elements comprise capacitors.

4. The structure of Claim 2, wherein circuit elements comprise transistors.

5. The structure of Claim 1, wherein capacitors and transistors are incorporated into the interposer.

6. The structure of Claim 1, further comprising a circuit substrate coupled to the second side of the interposer.

7. The structure of Claim 6, wherein the die is coupled to the interposer by solder bumps, and the interposer is coupled to the circuit substrate by solder balls.

8. The structure of Claim 7 wherein the solder bumps have a first pitch, the solder balls have a second pitch, and the second pitch is greater than the first pitch.

9. The structure of Claim 1, wherein the interposer has a first interconnection pitch on the first side, and a second interconnection pitch on the second side, and the second interconnection pitch is greater than the first interconnection pitch.

10. An assembly comprising:

an integrated circuit formed on a silicon substrate;

an interposer having a first surface and an opposing second surface; and

a circuit substrate;

wherein the interposer is disposed between the integrated circuit and the circuit substrate, and the interposer comprises silicon.

11. The assembly of the Claim 10, wherein the interposer is electrically and mechanically coupled to the integrated circuit.

12. The assembly of Claim 11, wherein the interposer is coupled to the integrated circuit by a plurality of solder bumps.

13. The assembly of Claim 11, wherein the interposer is coupled to the circuit substrate by a plurality of solder balls.

14. The assembly of Claim 10, further comprising electrical circuits incorporated into the interposer.

15. The assembly of Claim 14, wherein the electrical circuits comprise electrostatic discharge protection circuits.

16. The assembly of Claim 14, wherein the electrical circuits comprise buffer circuits.

17. The assembly of Claim 14, wherein the electrical circuits comprise memory circuits.

18. An electronic assembly comprising:

a die having a silicon substrate;

an interposer having a silicon substrate with a first surface and an opposing second surface, the first surface attached to the die by solder bumps; and

a circuit substrate attached to the second surface by sold r balls;

wherein the interposer comprises circuit elements.

19. The electronic assembly of Claim 18, wherein the circuit elements comprise active circuit elements.

20. The electronic assembly of Claim 18, wherein the circuit elements comprise passive circuit elements.

21. The electronic assembly of Claim 18, wherein the circuit elements comprise active and passive circuit elements.

22. The electronic assembly of Claim 21, wherein the active circuit elements include at least one field effect transistor, and the passive circuit elements include at least one capacitor.

23. The electronic assembly of Claim 18, wherein the die comprises a first plurality of insulated gate field effect transistors having a first set of electrical characteristics, the interposer comprises a second plurality of insulated gate field effect transistors having a second set of electrical characteristics, and the first set of electrical characteristics are different from the second set of electrical characteristics.

24. The electronic assembly of Claim 23, wherein the first set of electrical characteristics includes a first gate dielectric breakdown voltage, the second set of electrical characteristics includes a second gate dielectric breakdown voltage and the second gate dielectric breakdown voltage is greater than the first gate dielectric breakdown voltage.

25. The electronic assembly of Claim 18, wherein the die and the interposer are electrically coupled through the solder bumps, and a first power supply node of the die is coupled to a first terminal of a capacitor disposed on the interposer, and a second power supply node of the die is coupled to a second terminal of the capacitor.

26. A method of making an electronic assembly, comprising:

coupling an integrated circuit (IC) and an interposer; and

coupling a circuit substrate and the interposer;

wherein the IC and the interposer each have a body substantially comprising the same material, and wherein coupling comprises mechanically attaching and electrically connecting.

27. The method of Claim 26, wherein the IC and the interposer each have a body substantially comprising silicon, and wherein the circuit substrate comprises a printed circuit board.

28. The method of Claim 26, furth r comprising forming circuit elements on th interposer.

29. The method of Claim 26, further comprising incorporating circuit elements into the interposer.

30. The method of Claim 29, wherein circuit elements comprise active and passive circuit elements.

31. A method of making an interposer, comprising:

forming an oxide layer on each of a first surface and a second surface of a substrate;

patterning the oxide layer of the first surface so as to expose portions of the substrate;

isotropically etching through a first portion of the exposed substrate to form a first portion of a deep-via opening;

anisotropically etching through a second portion of the exposed substrate to form a second portion of a deep-via opening;

sputtering a copper barrier and a copper seed layer into the first and second portions of the deep-via opening;

electroplating a conductive material over the seed layer to form a deep-via; and

forming vias and interconnect lines over the second surfac of the substrate;

wherein at least one interconnect line is electrically coupled to at least one deep-via.